Parallel Plate Capacitance Calculator

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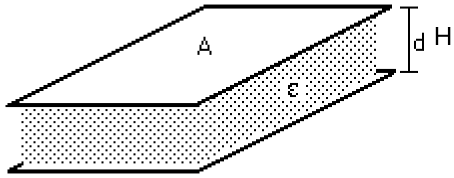
This sheet is used to calculate the capacitance obtained from Lee,The Design of CMOS Radio-Frequency Integrated Circuits
The Area (A) = W * L

$\mathbf{e}_r := 4.1$

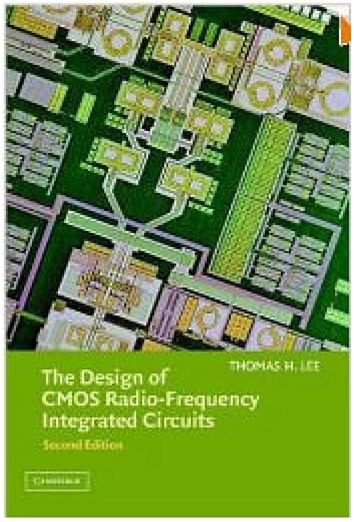
$$\mathbf{e}_o := 8.854187817\cdot 10^{-12}\cdot\frac{\text{farad}}{\text{m}}$$

$\text{fF} := 10^{-15}\text{F}$



Conventional

$$\text{CConventional}(W, L, H) := \frac{\mathbf{e}_r\cdot\mathbf{e}_o\cdot W\cdot L}{H}$$



Yuan's Formula

$$\text{CYuan}(W, L, T, H) := \mathbf{e}_r\cdot\mathbf{e}_o\left[\frac{W}{H} + \frac{2\cdot\mathbf{p}}{\ln\left[1 + \left(\frac{2\cdot H}{T}\right)\cdot\left(1 + \sqrt{1 + \frac{T}{H}}\right)\right]} - \frac{T}{2\cdot H}\right]\cdot L$$

Sakurai's Formula

$$\text{CSakurai}(W, L, T, H) := \mathbf{e}_r\cdot\mathbf{e}_o\cdot\left[\frac{W}{H} + 0.15\cdot\frac{W}{H} + 2.8\cdot\left(\frac{T}{H}\right)^{0.222}\right]\cdot L$$

Meijs & Fokkema Formula

$$CMF(W,L,T,H) := \mathbf{e}_r \cdot \mathbf{e}_o \cdot \left[\frac{W}{H} + 0.77 + 1.06 \cdot \left[\left(\frac{W}{H} \right)^{0.25} + \left(\frac{T}{H} \right)^{0.5} \right] \right] \cdot L$$

$CMF(1.36m, 1m, 0.8m, 1.65m) = 1.213 \times 10^{-10} F$

$CSakurai(1.36m, 1m, 0.8m, 1.65m) = 1.21 \times 10^{-10} F$

$CYuan(1.36m, 1m, 0.8m, 1.65m) = 1.195 \times 10^{-10} F$

$CConventional(1.36m, 1m, 1.65m) = 2.992 \times 10^{-11} F$

$CMF(2.38m, 1m, 0.3m, 0.87m) = 1.993 \times 10^{-10} F$

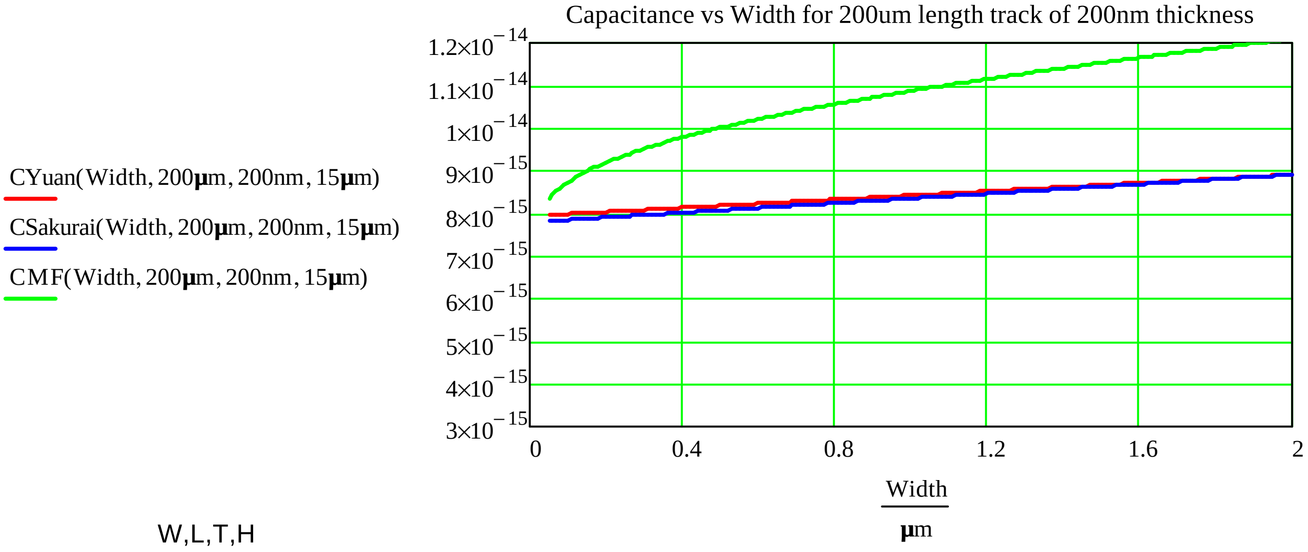
$CSakurai(2.38m, 1m, 0.3m, 0.87m) = 1.945 \times 10^{-10} F$

$CYuan(2.38m, 1m, 0.3m, 0.87m) = 1.806 \times 10^{-10} F$

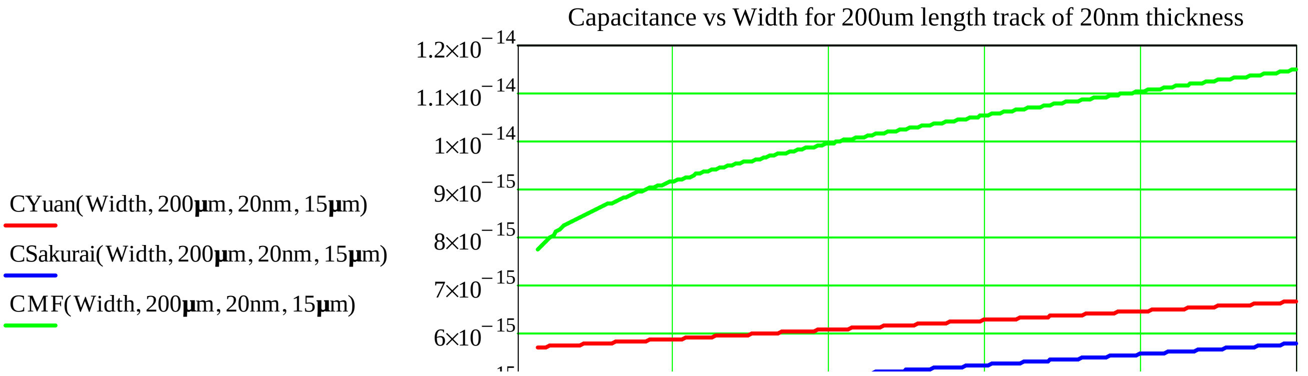
$CConventional(2.38m, 1m, 0.87m) = 9.931 \times 10^{-11} F$

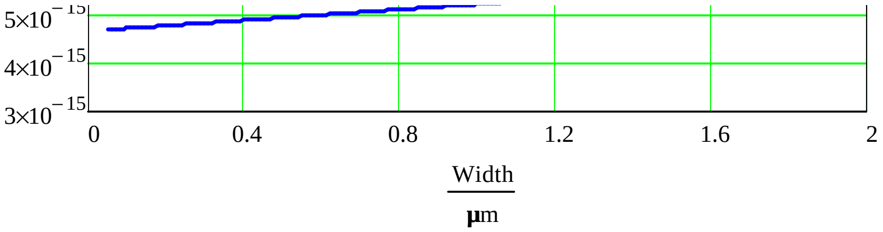
This graph shows the capacitance for a 200um long track, spaced 15um above the ground and of various widths
These two graphs are for different track thicknesses and are not as close in agreement as I was expecting!!!

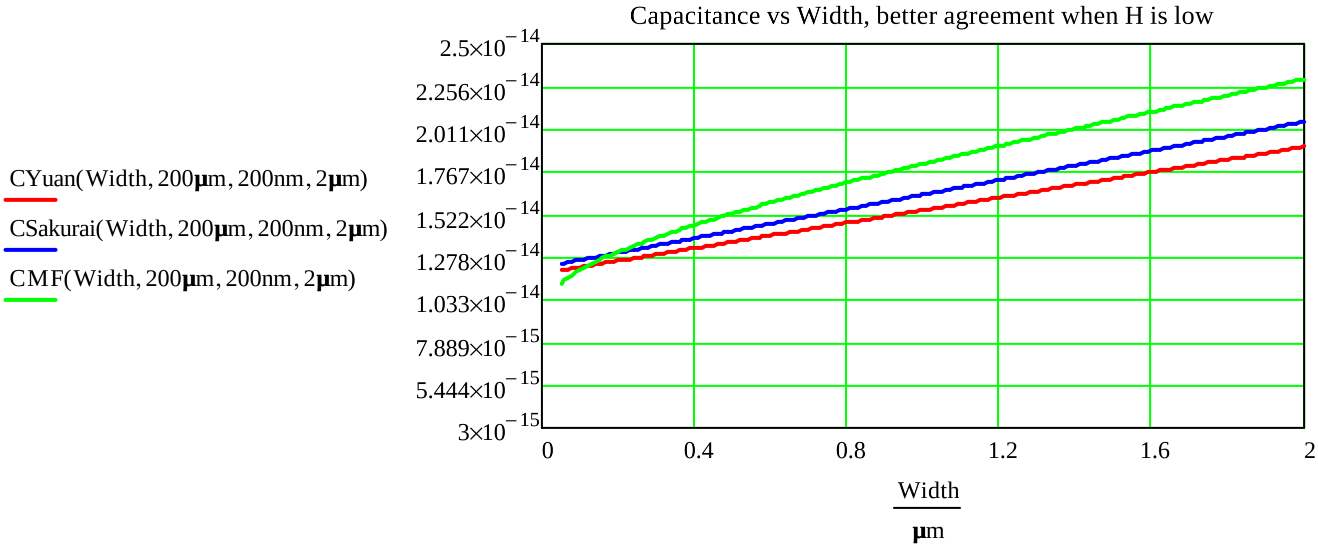
$Width := 0.05 \cdot \mu m, 0.06 \cdot \mu m .. 2 \cdot \mu m$



W,L,T,H




5×10^−15
4×10^−15
3×10^−15
0
0.4
0.8
1.2
1.6
2
Width / µm


Capacitance vs Width, better agreement when H is low
CYuan(Width, 200µm, 200nm, 2µm)
CSakurai(Width, 200µm, 200nm, 2µm)
CMF(Width, 200µm, 200nm, 2µm)
2.5×10^−14
2.256×10^−14
2.011×10^−14
1.767×10^−14
1.522×10^−14
1.278×10^−14
1.033×10^−14
7.889×10^−15
5.444×10^−15
3×10^−15
0
0.4
0.8
1.2
1.6
2
Width / µm

At radio frequencies, it becomes especially crucial to obtain accurate values for the parasitic capacitance of interconnect. The parallel plate formula from undergraduate physics often grossly underestimates the capacitance because one dimension is often not much larger than the distance to the next conductor layer. The fringing capacitance is therefore significant, and the simple formula is often unacceptably inaccurate.

We will consider three configurations of conductors: Case 1 is a single wire over a conducting plane of infinite extent; Case 2 is a single wire between two infinite planes; and Case 3 is a wire between two adjacent wires all over a single infinite plane. Those who are uninterested in the somewhat tedious derivations may skip to the summary of the formulas. Finally, keep in mind that, in all cases considered here, a uniform dielectric is assumed. The presence of passivation layers and/or plastic packaging typically increases the capacitance by amounts ranging from about 10% for the topmost layers of interconnect to only 1–2% for the innermost layers.

Case 1: Single Conductor over Ground Plane

The case of a single, isolated wire over a conducting plane is perhaps the easiest one to consider first. One formula for this case, offered by Yuan,[6] has an intuitive appeal because it is physically motivated: it explicitly decomposes the capacitance into area and fringe terms by modeling progressively as shown in Figure 2.5 (we assume that the wire is infinitely long along the direction perpendicular to the plane of this page).

[6] C. P. Yuan and T. N. Trick, "A Simple Formula for the Estimation of the Capacitance of Two-Dimensional Interconnects in VLSI Circuits," *IEEE Electron Device Lett.*, v. EDL-3, 1982, pp. 391–3.

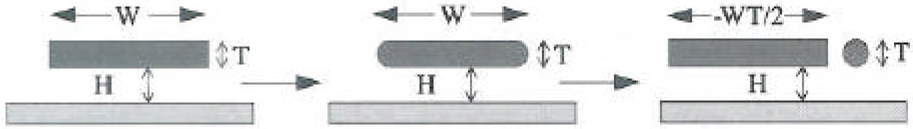


FIGURE 2.5. Yuan's decomposition of parallel plate capacitance into area and fringe components.

As seen in the figure, the basic idea is to obtain the total capacitance as the sum of two parts. One component is the familiar area (fringeless) term proportional to W/H, while the other (fringe) contribution involves the capacitance due to a wire of diameter T, diminished by the term proportional to $T/2H$. Yuan's formula for the capacitance per unit length is thus

$$C_{\text{Yuan}} \approx \varepsilon\left[\frac{W}{H} + \frac{2\pi}{\ln\{1 + (2H/T)(1 + \sqrt{1 + T/H})\}} - \frac{T}{2H}\right]. \tag{8}$$

Yuan's approach works well as long as the ratio W/H is not too small, with typical errors in the range of 5% or so.[7] Below W/H values of about 2–3, however, the error grows quite rapidly. Unfortunately, that often can be the regime of interest, particularly when future process technologies are considered. Also, the subexpression for the fringe capacitance is still a bit cumbersome.

Another strategy is to abandon any physically motivated approach and directly apply function-fitting techniques to the results of two-dimensional (2D) field-solver simulations. One formula resulting from such an exercise was developed by Sakurai:[8]

$$C_{\text{Sakurai}} \approx \varepsilon\left[\frac{W}{H} + \frac{0.15W}{H} + 2.8\left(\frac{T}{H}\right)^{0.222}\right], \tag{9}$$

where the area contribution (first term) and fringe contribution (other two terms) are shown separately, as before.

As with Yuan's formula, Sakurai's equation has increasingly poor accuracy at large W/H ratios, but accuracy superior to Yuan's at small W/H, with the accuracy of the equations crossing over in the neighborhood of $W/H = 2$–3, at least for the particular values of conductor and dielectric thicknesses considered in Barke's paper ($T = 1.3\ \mu\text{m}$, $H = 0.75\ \mu\text{m}$).

Better accuracy can be obtained with a formula that is only marginally more complex (although possibly an increment more computationally efficient) than Sakurai's.

[7] E. Barke, "Line-to-Ground Capacitance Calculation for VLSI: A Comparison," *IEEE Trans. Computer-Aided Design*, v. 7, no. 2, February 1988, pp. 295–8.

[8] T. Sakurai and K. Tamaru, "Simple Formulas for Two- and Three-Dimensional Capacitances," *IEEE Trans. Electron Devices*, v. ED-30, no. 2, February 1983, pp. 183–5.

Table 2.1. *Capacitance of single wire over single conducting plane*

Method	Capacitance for $W = 1.36$, $H = 1.65$, $T = 0.8$	Capacitance for $W = 2.38$, $H = 0.87$, $T = 0.3$
MF	0.115	0.190
Sakurai	0.115	0.185
Yuan	0.114	0.172

[illegible]	[illegible]	[illegible]
Area term	0.028	0.094

Such an equation, developed by v.d. Meijs and Fokkema (hereafter referred to as MF) through function fitting, is:[9]

$$C_{\mathrm{MF}} \approx \varepsilon \left[\frac{W}{H} + 0.77 + 1.06 \left[\left(\frac{W}{H} \right)^{0.25} + \left(\frac{T}{H} \right)^{0.5} \right] \right]. \tag{10}$$

Barke claims that the MF formula typically yields accuracies better than 1% for dimensions appropriate to ICs. The simplicity and accuracy of the MF formula are very attractive (requiring only the availability of a square-root extractor in addition to the usual arithmetic functions). Additionally, as we'll see, the MF formula is a nice basic equation from which formulas for other cases may evolve.